

FPGA Verification & Validation Engineer

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Company: QuEST Global Services Pte. Ltd

Location: Poland

Category: architecture-and-engineering

Quest Global is an organization at the forefront of innovation and one of the world's fastest growing engineering services firms with deep domain knowledge and recognized expertise in the top OEMs across seven industries. We are a twenty-five-year-old company on a journey to becoming a centenary one, driven by aspiration, hunger and humility.

We are looking for humble geniuses, who believe that engineering has the potential to make the impossible, possible; innovators, who are not only inspired by technology and innovation, but also perpetually driven to design, develop, and test as a trusted partner for Fortune 500 customers.

As a team of remarkably diverse engineers, we recognize that what we are really engineering is a brighter future for us all. If you want to contribute to meaningful work and be part of an organization that truly believes when you win, we all win, and when you fail, we all learn, then we're eager to hear from you.

The achievers and courageous challenge-crushers we seek, have the following characteristics and skills:

Job Overview:

EXB Solutions is currently participating in the testing of an aerospace data manager device and is seeking FPGA UVM Verification Engineers.

This Engineer will be joining the existing team who is establishing the UVM (Universal Verification Methodology) environment and is a seasoned group of engineers:

Verification experience

Needs to have a good working knowledge of UVM, in the area of script development

Must be self-motivated and have a lot of initiative to reach out and interact with the existing team

Individual that has working knowledge of digital systems, and components, FPGA design methodologies, testing, debugging, root causing and testing methodologies.

Experience with DO254 Dal A development

Required Skills:

Ability to Construct FPGA Test Bench using UVM Components.

System Verilog

Sequence Development

Developing DO254 related documents including but not limited to: Test Plans, Test Procedures, Test Cases, Maintaining a Trace Matrix

Troubleshooting RTL Design Flaws using Simulation Environment.

Ability to take a problem and come up with a solution.

Familiarity with Unit level testbenches

Familiarity with Chip Level testbenches

Preferred Skills:

Develop UVM Predictors and Scoreboards to Implement Self-Checking Simulation Tests.

Familiarity with Register Modeling and Predicting Register Behavior.

Proficiency in developing UVM Agents, Drivers, Monitors, and Sequence Items.

Code Coverage Analysis for RTL Source (Statement, Branch, FSM, FSM Transition)

Technologies & Tools:

SVN

Mentor Graphics Questasim

Verilog

VHD

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